

Claims

- [c1] A method for generating a silicide resistor in one of a plurality of back-end-of-line (BEOL) layers without using high temperature processing, the method comprising the steps of:
- forming a trough in an inter-layer dielectric (ILD) layer of the plurality of BEOL layers;
 - depositing a polysilicon layer over the trough;
 - etching the polysilicon layer to have a top surface below a surface of the ILD layer within the trough to form a polysilicon base in the trough;
 - depositing a first metal;
 - annealing to form a silicide layer from the first metal;
 - and
 - planarizing to form a silicide section within the trough to generate the silicide resistor.
- [c2] The method of claim 1, wherein the trough forming step includes patterning the ILD layer and etching to form the trough.
- [c3] The method of claim 1, wherein the ILD layer includes one of: silicon dioxide (SiO₂), SiLK, boron doped oxide, and a high-k dielectric.

- [c4] The method of claim 1, further comprising the step of forming one of a via through the ILD layer, and a wire in the ILD layer.
- [c5] The method of claim 1, wherein an anneal temperature is lower than a damaging temperature that would damage a structure in the plurality of BEOL layers.
- [c6] The method of claim 1, wherein the first metal is one of: cobalt (Co), palladium (Pd), platinum (Pt), nickel (Ni), molybdenum (Mo) and tungsten (W).
- [c7] The method of claim 1, further comprising the step of forming a contact to the silicide section.
- [c8] The method of claim 1, wherein the silicide section includes palladium silicide (PdSi) and has a resistivity of no less than approximately 25 μ -ohms/cm and no greater than approximately 30 μ -ohms/cm.
- [c9] The method of claim 1, wherein the silicide section includes platinum silicide (PtSi) and has a resistivity of no less than approximately 26 μ -ohms/cm and no greater than approximately 35 μ -ohms/cm.
- [c10] The method of claim 1, wherein the silicide section includes nickel silicide (NiSi) and has a resistivity of no less than approximately 14 μ -ohms/cm and no greater than

approximately 20 μ -ohms/cm.

- [c11] The method of claim 1, wherein the silicide section include di-nickel silicide (Ni_2Si) and has a resistivity of no less than approximately 35 μ -ohms/cm and no greater than approximately 50 μ -ohms/cm.
- [c12] A resistor for a semiconductor device, the resistor comprising:
a silicide section positioned in one of a plurality of back-end-of-line (BEOL) layers;
wherein the silicide section has a silicidation temperature less than a damaging temperature of the plurality of BEOL layers.
- [c13] The resistor of claim 12, wherein the silicide section includes cobalt silicide (CoSi) and has a resistivity of no less than approximately 14 μ -ohms/cm and no greater than approximately 20 μ -ohms/cm.
- [c14] The resistor of claim 12, wherein the silicide section includes palladium silicide (PdSi) and has a resistivity of no less than approximately 25 μ -ohms/cm and no greater than approximately 30 μ -ohms/cm.
- [c15] The resistor of claim 12, wherein the silicide section includes platinum silicide (PtSi) and has a resistivity of no less than approximately 26 μ -ohms/cm and no greater

than approximately 35 μ -ohms/cm.

- [c16] The resistor of claim 12, wherein the silicide section includes nickel silicide (NiSi) and has a resistivity of no less than approximately 14 μ -ohms/cm and no greater than approximately 20 μ -ohms/cm.
- [c17] The resistor of claim 12, wherein the silicide section includes di-nickel silicide (Ni_2Si) and has a resistivity of no less than approximately 35 μ -ohms/cm and no greater than approximately 50 μ -ohms/cm.
- [c18] The resistor of claim 12, wherein the silicide section includes one of molybdenum silicide (MoSi_2) and tungsten silicide (WSi_2).
- [c19] The resistor of claim 12, further comprising a polysilicon base positioned below the silicide section.
- [c20] A semiconductor device comprising:
a silicide resistor in one of a plurality of back-end-of-line (BEOL) layers, the silicide resistor including a silicide section having a silicidation temperature less than a damaging temperature of the plurality of BEOL layers.